AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multiplexer circuit, comprising:

a first plurality of circuit input terminals providing a first plurality of input signals;

a second plurality of circuit input terminals providing a second plurality of input signals having complementary values to the first plurality of input signals;

a circuit output terminal;

a first multiplexer having a plurality of input terminals coupled to the first plurality of circuit input terminals, at least one select terminal, and an output terminal;

a second multiplexer having a plurality of input terminals coupled to the second plurality of circuit input terminals, at least one select terminal coupled to the at least one select terminal of the first multiplexer, and an output terminal; [[and]]

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the circuit output terminal; and

a plurality of inversion circuits, each inversion circuit being coupled between one of the first circuit input terminals and a corresponding one of the second circuit input terminals, each inversion circuit comprising a memory cell,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

Claim 2. (Cancelled)

3. (Currently Amended) The multiplexer circuit of Claim [[2]] 1, wherein each of the inversion circuits further comprises an inverter.

Claims 4-5. (Cancelled)

6. (Currently Amended) The multiplexer circuit of Claim 1, ~~further comprising a plurality of memory cells,~~ wherein each memory cell ~~having~~ comprises a true output terminal coupled to one of the first plurality of circuit input terminals and a complement output terminal coupled to a corresponding one of the second plurality of circuit input terminals.

7. (Original) The multiplexer circuit of Claim 1, further comprising at least one memory cell coupled to the select terminals of the first and second multiplexers.

8. (Original) The multiplexer circuit of Claim 1, wherein:

each of the first and second multiplexers comprises a plurality of select terminals comprising select terminal pairs; and

the multiplexer circuit further comprises, for each select terminal pair, an inverter coupled between the two select terminals comprising the pair.

9. (Original) The multiplexer circuit of Claim 1, wherein the output circuit comprises a latch.

10. (Original) The multiplexer circuit of Claim 9, wherein the latch comprises first and second cross-coupled inverters.

11. (Original) The multiplexer circuit of Claim 1, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the first multiplexer and an output terminal coupled to the circuit output terminal;

a first pullup coupled between the output terminal of the first multiplexer and a power high terminal, the first pullup having a gate terminal coupled to the output terminal of the second multiplexer; and

a second pullup coupled between the output terminal of the second multiplexer and the power high terminal, the second pullup having a gate terminal coupled to the output terminal of the first multiplexer.

12. (Original) The multiplexer circuit of Claim 1, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the second multiplexer and an output terminal coupled to the output terminal of the first multiplexer; and

a P-channel transistor coupled between the output terminal of the second multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer and further coupled to the circuit output terminal.

13. (Original) The multiplexer circuit of Claim 1, wherein the first and second pluralities of circuit input terminals each comprise eight input terminals.

14. (Original) The multiplexer circuit of Claim 1, wherein the first and second multiplexers each comprise a plurality of transistors coupled in series between their respective input and output terminals, and all of the transistors consist of N-channel transistors.

15. (Original) The multiplexer circuit of Claim 1, wherein the first and second multiplexers comprise binary multiplexers.

16. (Original) The multiplexer circuit of Claim 1, wherein the first and second multiplexers comprise one-hot multiplexers.

Claims 17-60. (Cancelled)